Data Sheet | March 25, 2008 | FN6340.3

6A Dual Synchronous Buck Regulator with Integrated MOSFETs

The ISL65426 is a high efficiency dual output monolithic synchronous buck converter operating over an input voltage range of 3V to 5.5V. This single chip power solution provides two output voltages, which are selectable or externally adjustable from 1V to 80% of the supply voltage while delivering up to 6A of total output current. The two PWMs are synchronized 180° out-of-phase, reducing the RMS input current and ripple voltage.

The ISL65426 switches at a fixed frequency of 1MHz and utilizes current-mode control with integrated compensation to minimize the size and number of external components and provide excellent transient response. The internal synchronous power switches are optimized for good thermal performance and high efficiency.

A unique power block architecture allows partitioning of six 1A blocks to support one of four configuration options. One master power block is associated with each synchronous converter channel. Four floating slave power blocks allow the user to assign them to either channel. Proper external configuration of the power blocks is verified internally prior to soft-start initialization.

Independent enable inputs allow for synchronization or sequencing soft-start intervals of the two converter channels. A third enable input allows additional sequencing for multi-input bias supply designs. Individual power-good indicators (PG1, PG2) signal when output voltage is within the regulation window.

The ISL65426 integrates protection for both synchronous buck regulator channels. The fault conditions include overcurrent, undervoltage, and IC thermal monitor.

High integration contained in a thin Quad Flat No-lead (QFN) package makes the ISL65426 an ideal choice to power many of today's small form factor applications. A single chip solution for large scale digital ICs, like field programmable gate arrays (FPGA), requiring separate core and I/O voltages.

Features

- High Efficiency: Up to 95%
- Fixed Frequency: 1MHz
- Operates From 3V to 5.5V Supply
- ±1% Reference
- Flexible Output Voltage Options
  - Programmable 2-Bit VID Input
  - Adjustable Output From 1V to 4.0V
- User-Partitioned Power Blocks
- Ultra-Compact DC/DC Converter Design
- PWMs Synchronized 180° Out-of-Phase
- Independent Enable Inputs and System Enable
- Stable All Ceramic Solutions
- Excellent Dynamic Response
- Independent Output Digital Soft-Start
- Power-Good Output Voltage Monitor
- Thermal-Overload Protection
- Overcurrent and Undervoltage Protection
- Pb-Free (RoHS Compliant)

Applications

- FPGA, CPLD, DSP, and CPU Core and I/O Voltages
  - Xilinx Spartan III™, Virtex II™, Virtex II Pro™, Virtex 4™
  - Altera Stratix™, Stratix II™, Cyclone™, Cyclone II™
  - Actel Fusion™, LatticeSC™, LatticeEC™
- Low-Voltage, High-Density Distributed Power Systems
- Point-of-Load Regulation
- Distributed Power Systems
- Set-Top Boxes

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL65426HRZ*	ISL65426 HRZ	-10 to +100	50 Ld 5x10 QFN	L50.5x10
ISL65426IRZA*	ISL65426 IRZ	-40 to +85	50 Ld 5x10 QFN	L50.5x10

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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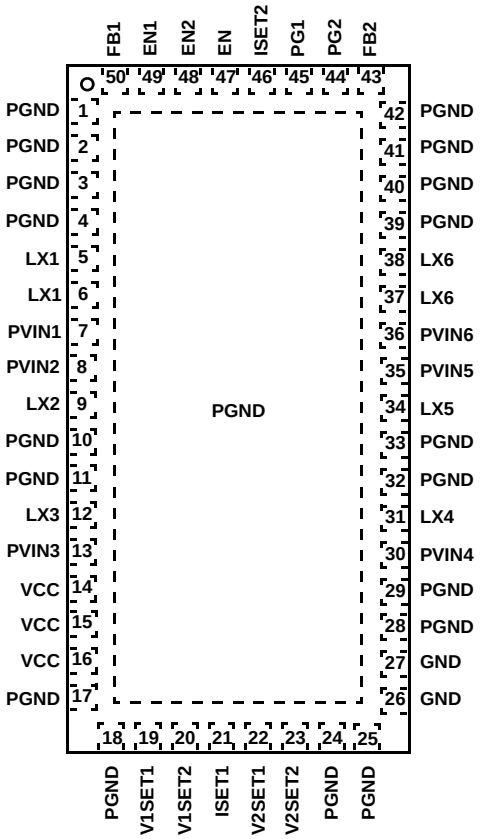
Pinout

ISL65426
(50 LD QFN)
TOP VIEW



Typical Application Schematics

SINGLE INPUT SUPPLY

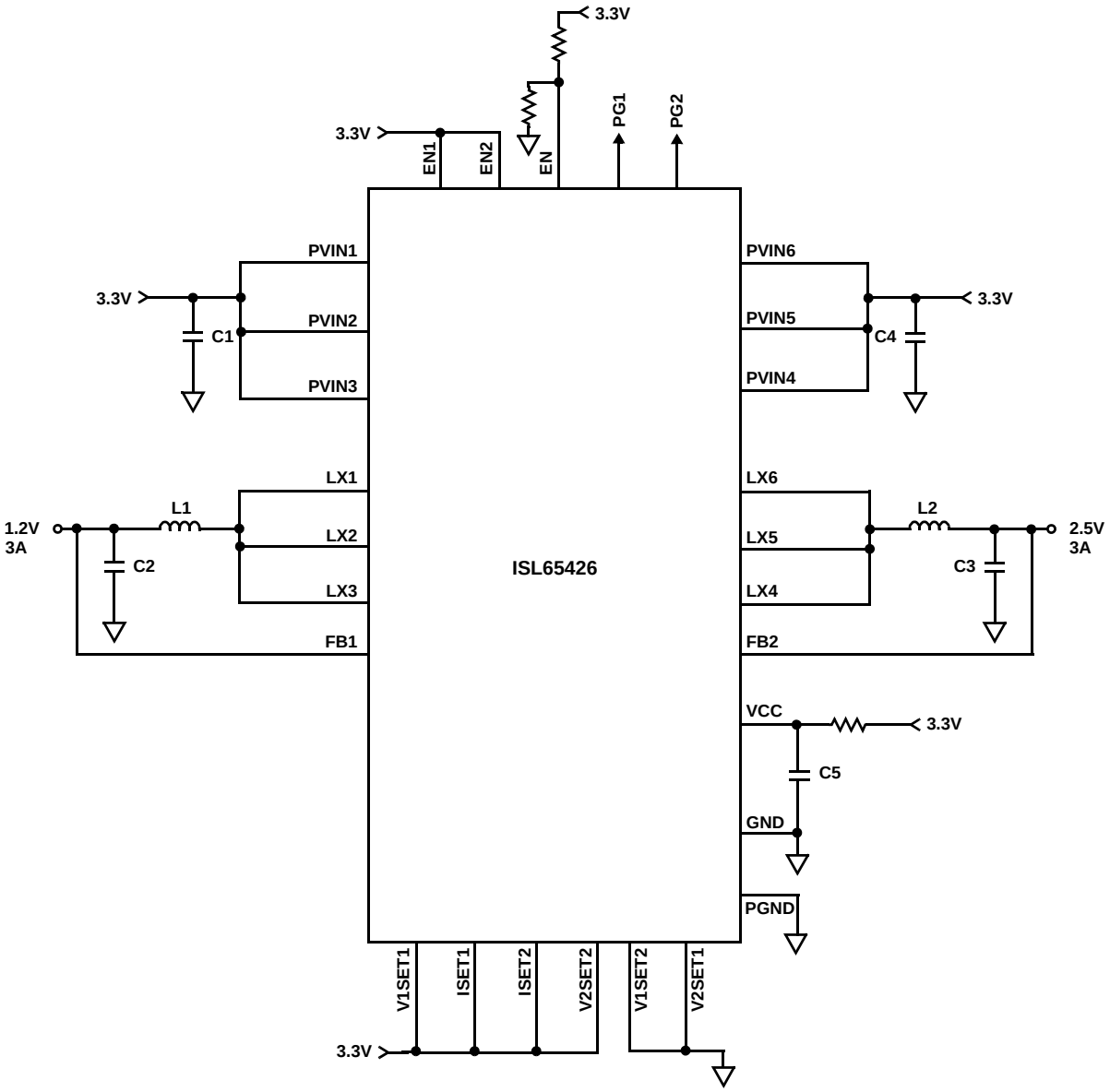


FIGURE 1. TYPICAL APPLICATION FOR 3A:3A CONFIGURATION

Typical Application Schematics (Continued)

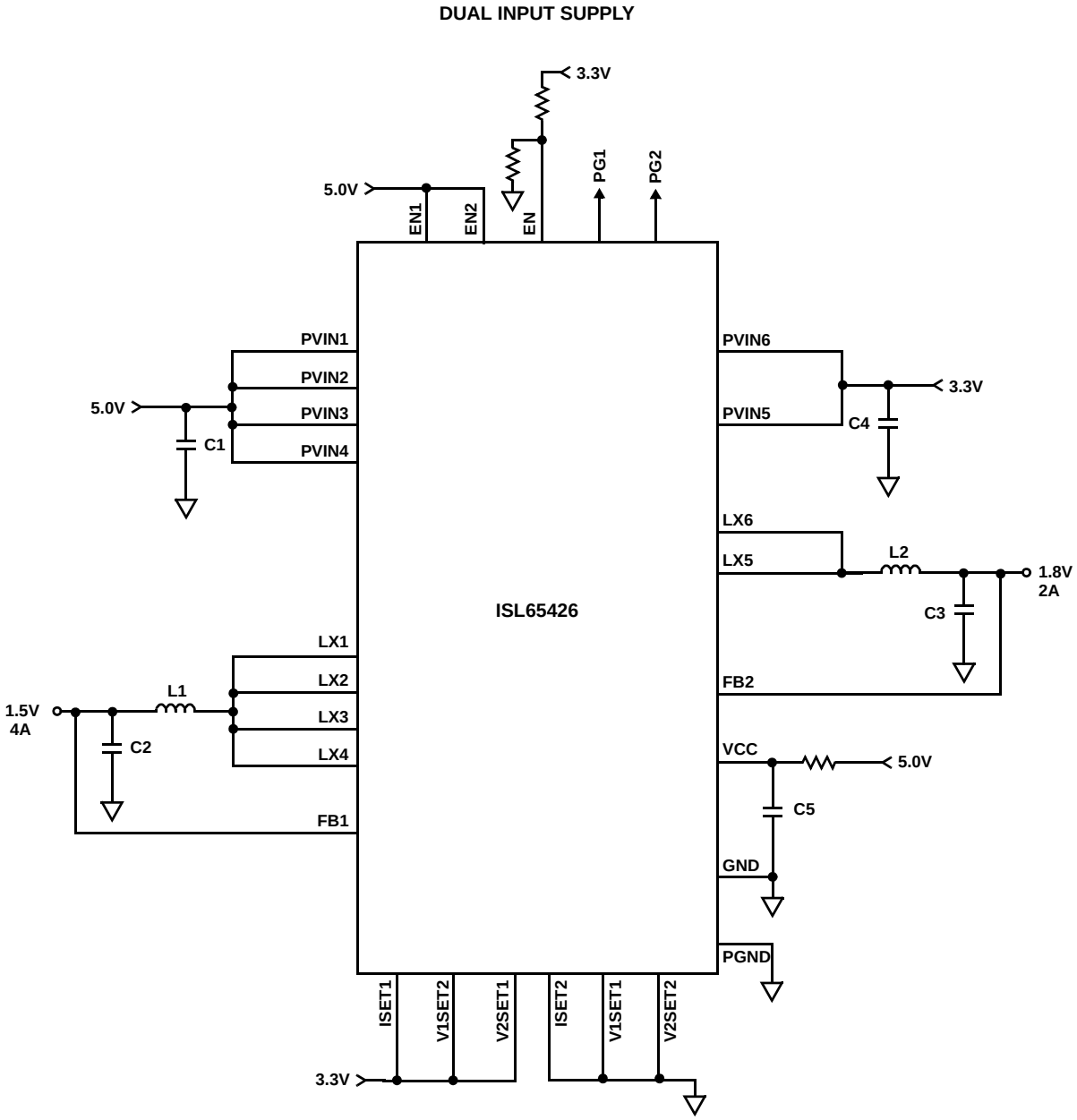


FIGURE 2. TYPICAL APPLICATION FOR 4A:2A CONFIGURATION

Typical Application Schematics (Continued)

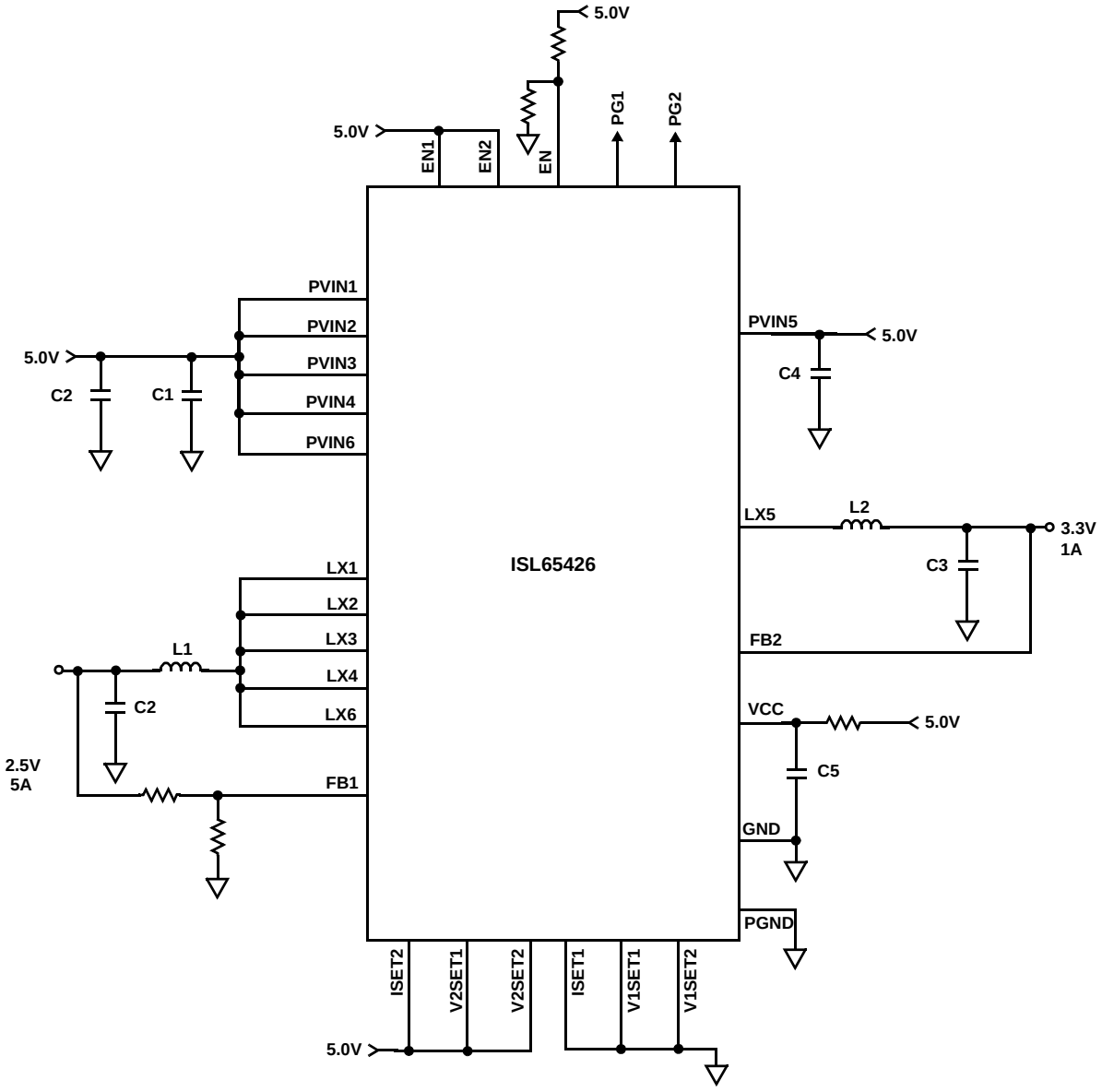
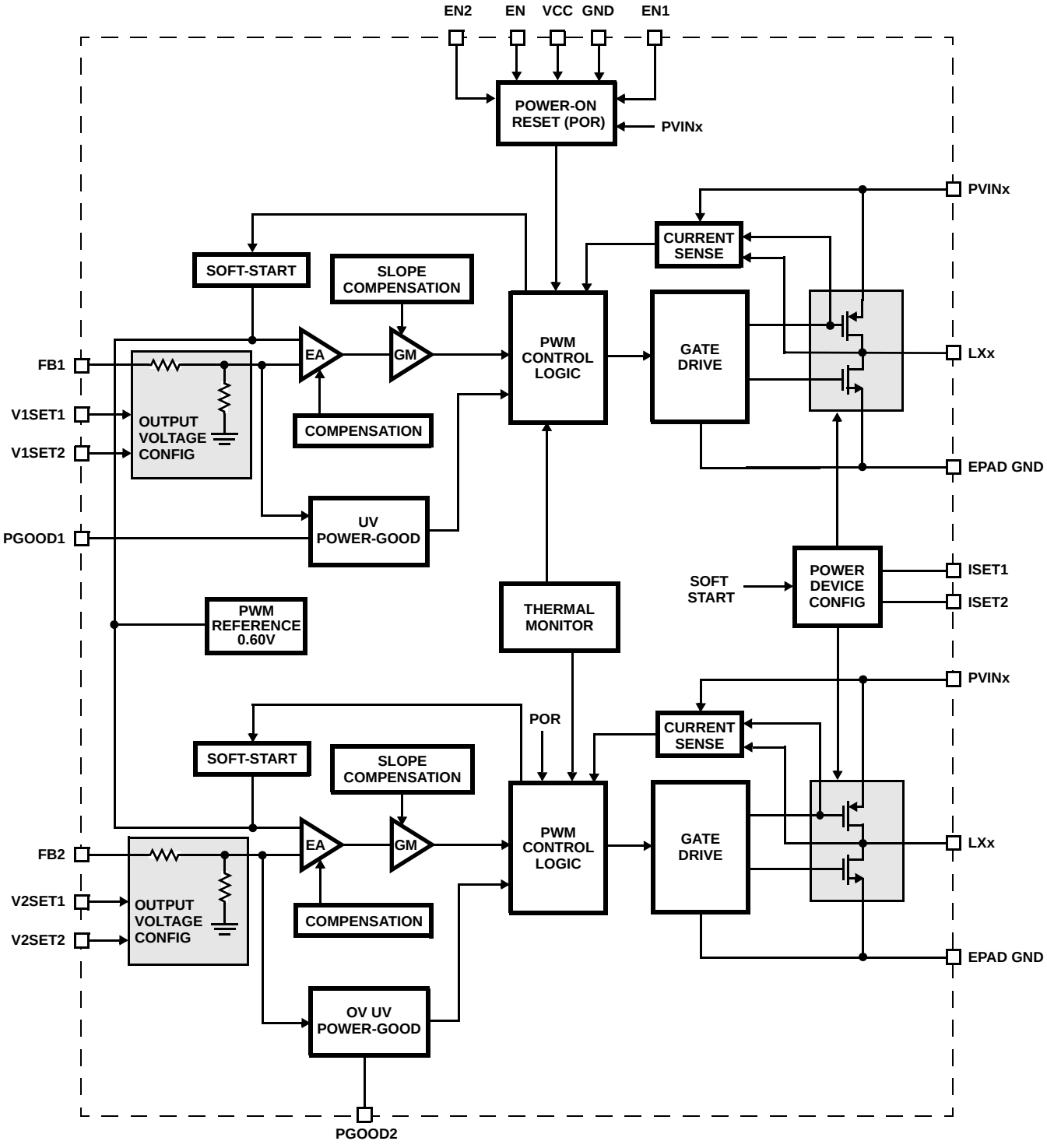


FIGURE 3. TYPICAL APPLICATION FOR 5A:1A CONFIGURATION

Functional Block Diagram



Absolute Maximum Ratings

VCC, PVINx, LXx . . . . . GND - 0.3V to +6V
FBx, ENx, VxSETx, ISETx, PGOODx . . . . . -0.3V to VCC + 0.3V

Recommended Operating Input Range

VCC, PVINx . . . . . 3V to +5.5V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
50 Ld QFN Package (Notes 1, 2)	23	2.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range (ISL65426HRZ) . . . . -10°C to +100°C
Ambient Temperature Range (ISL65426IRZA) . . . . . -40°C to +85°C
Operating Junction Temperature Range . . . . . -10°C to +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside. See Tech Brief TB379 for details.

Electrical Specifications

Recommended operating conditions, unless otherwise noted. VCC = PVIN = 5.0V, T_A = -10°C to +100°C for ISL65426HRZ and T_A = -40°C to +85°C for ISL65426IRZA. (Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Quiescent Supply Current	EN1 = EN2 = EN = VCC = 5V, I_{OUT1} = I_{OUT2} = 0mA		30		mA
Shutdown Supply Current	EN1 = EN2 = EN = GND, VCC = PVIN = 5.5V		5.4	7	mA
	EN1 = EN2 = EN = GND, VCC = PVIN = 3.3V		2.8	3.2	mA
PHASE CONFIGURATION					
LX Pull-Down	LX1, LX3, LX4, LX5, LX6 Only - Configuration Only		1		mA
LX Output Leakage	Low Level, Single LX Output	-5		5	µA
	High Level, Single LX Output	-5		5	µA
Minimum Controllable ON-time	(Note 3)		125		ns
OUTPUT VOLTAGE TOLERANCE					
Reference Voltage Tolerance	T_J = -40°C to +100°C	0.594	0.6	0.606	V
	T_J = 100°C to +125°C	0.591	0.6	0.609	V
Programmed Output Voltage Tolerance	T_J = -40°C to +125°C; No Load	-2		+2	%
	T_J = -40°C to +125°C (Note 4); Full Load		±5		%
OSCILLATOR					
Accuracy		0.8	1	1.2	MHz
Maximum LX Pulse Width			950		ns
Minimum LX Pulse Width			50		ns
OUTPUT VOLTAGE SELECTION					
VxSETx Input High Threshold		0.4	1.2	1.5	V
VxSETx Pull-down		7	10	15	µA
POWER BLOCKS					
ISETx Input High Threshold		0.4	1.2	1.5	V
ISETx Pull-up		7	10	15	µA
Output Current	Per Block; VCC = PVIN = 5.0V; VOUT = 1.8V (Note 3)			1	A
	Per Block; VCC = PVIN = 3V; VOUT = 1.2V (Note 3)			0.7	A
Peak Output Current Limit	Per Block		2.0		A

Electrical Specifications Recommended operating conditions, unless otherwise noted. VCC = PVIN = 5.0V, T_A = -10°C to +100°C for ISL65426HRZ and T_A = -40°C to +85°C for ISL65426IRZA. (Note 5) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Upper Device $r_{DS(ON)}$	0.4A Per Block, VCC = PVIN = 3.3V, VOUT = 1.8V	60	100	140	mΩ
Lower Device $r_{DS(ON)}$	0.4A Per Block, VCC = PVIN = 3.3V, VOUT = 1.8V	30	55	85	mΩ
Efficiency	0.5A Per Block, VCC = PVIN = 3.3V, VOUT = 1.1V		90		%
	0.5A Per Block, VCC = PVIN = 5V, VOUT = 2.5V		95		%
POWER-ON RESET AND ENABLE PINS					
VCC POR Threshold	VCC Rising; No Load	2.15	2.25	2.35	V
	VCC Falling; No Load	2.05	2.15	2.25	V
PVIN POR Threshold	PVIN Rising; No Load	1.9	2.05	2.15	V
	PVIN Falling; No Load	1.75	1.90	2.00	V
PVIN Bias Output Voltage Enable Threshold	VOUT2 = 3.3V; VCC = PVIN	4.1	4.3	4.5	V
	VOUT2 = 2.5V; VCC = PVIN	2.8	2.9	3.0	V
EN1/EN2 Threshold	Rising Threshold; VCC = 5V	1.0	1.2	1.45	V
	Hysteresis		280		mV
	Rising Threshold; VCC = 3.3V	0.75	0.98	1.20	V
	Hysteresis		200		mV
	Rising Threshold; VCC = 3V	0.55	0.82	1.05	V
	Hysteresis		185		mV
EN1/EN2 Pull-up		7	10	15	µA
EN Threshold		0.57	0.6	0.63	V
EN Sink Current	EN = GND	7	11	15	µA
Soft-Start Time			4		ms
POWER-GOOD SIGNAL					
Rising Threshold	As % of VREF; V_{OUT1} = 1.8V; V_{OUT2} = 3.3V	110	115	120	%
Rising Hysteresis	As % of VREF; V_{OUT1} = 1.8V; V_{OUT2} = 3.3V	5	7	9	%
Falling Threshold	As % of VREF; V_{OUT1} = 1.8V; V_{OUT2} = 3.3V	80	85	90	%
Falling Hysteresis	As % of VREF; V_{OUT1} = 1.8V; V_{OUT2} = 3.3V	4	7	9	%
Power-Good Drive	VCC = 5V; PG1 = PG2 = 0.4V	1			mA
Power-Good Leakage				1	µA
PROTECTION FEATURES					
Undervoltage Monitor					
Undervoltage Trip Threshold	As % of VREF	70	75	80	%
Undervoltage Recovery Threshold	As % of VREF	82	89	95	%
THERMAL MONITOR					
Thermal Shutdown Temperature (Note 3)			150		°C

NOTES:

3. Limits should be considered typical and are not production tested.
4. Accounts for output variations due to jitter, which is a function of the input voltage and output loading.
5. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 5V, I_{OUT1} = 4A, I_{OUT2} = 2A, T_A = -10°C to +100°C unless otherwise noted. Typical values are at T_A = +25°C.

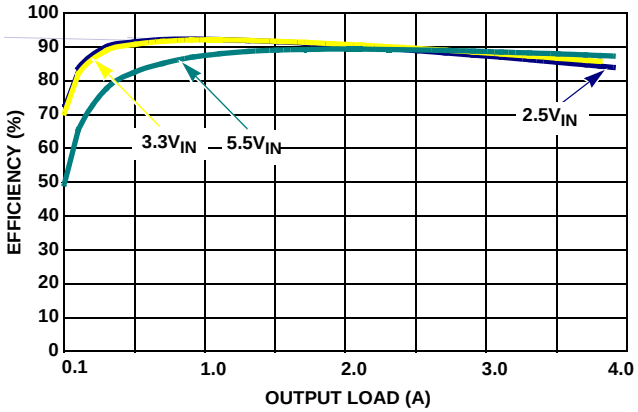


FIGURE 4. V_{OUT1} = 1.2V EFFICIENCY vs LOAD

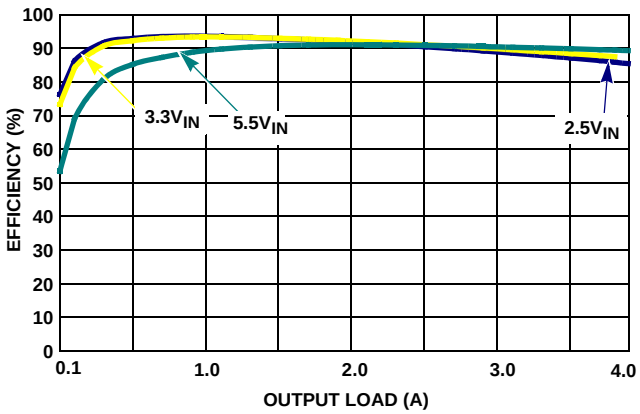


FIGURE 5. V_{OUT1} = 1.5V EFFICIENCY vs LOAD

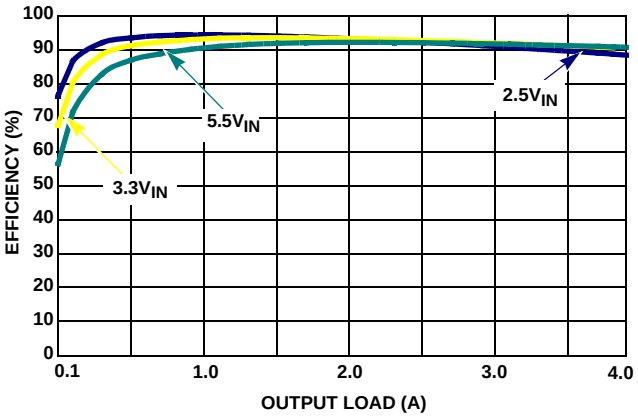


FIGURE 6. V_{OUT1} = 1.8V EFFICIENCY vs LOAD

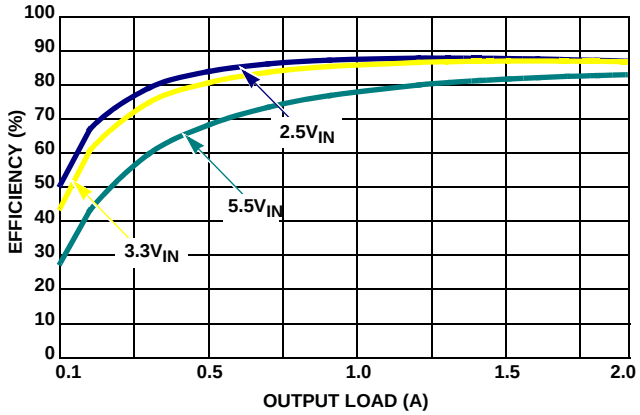


FIGURE 7. V_{OUT2} = 1.8V EFFICIENCY vs LOAD

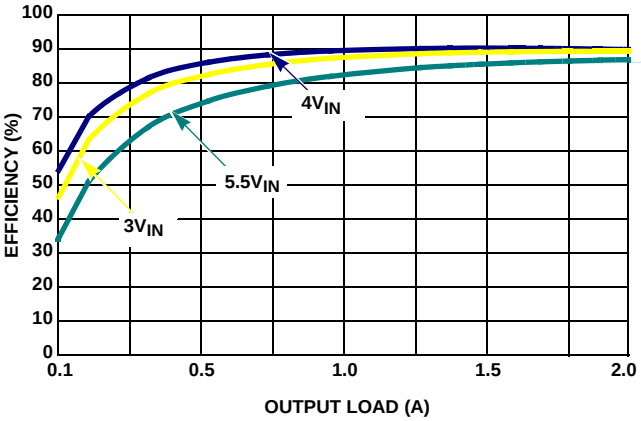


FIGURE 8. V_{OUT2} = 2.5V EFFICIENCY VS LOAD

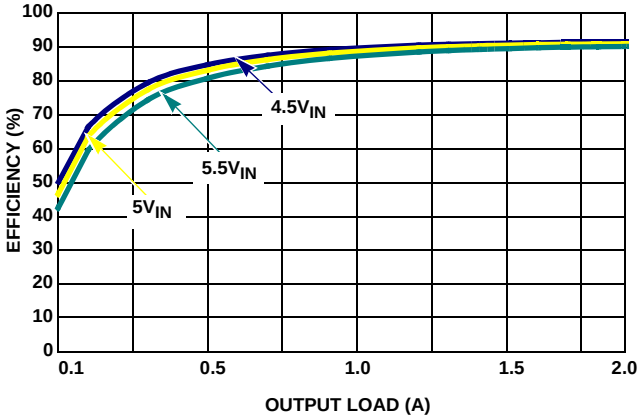


FIGURE 9. V_{OUT2} = 3.3V EFFICIENCY vs LOAD

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 5V, I_{OUT1} = 4A, I_{OUT2} = 2A, T_A = -10°C to +100°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

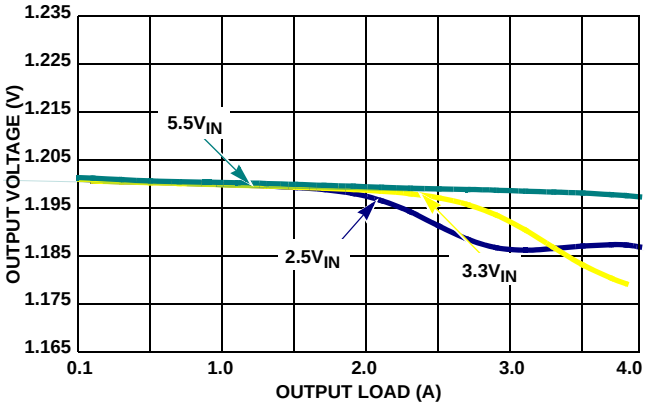


FIGURE 10. V_{OUT1} = 1.2V REGULATION vs LOAD

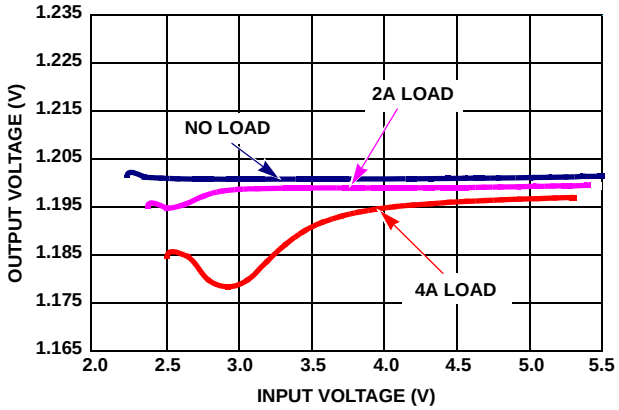


FIGURE 11. V_{OUT1} = 1.2V REGULATION vs V_{IN}

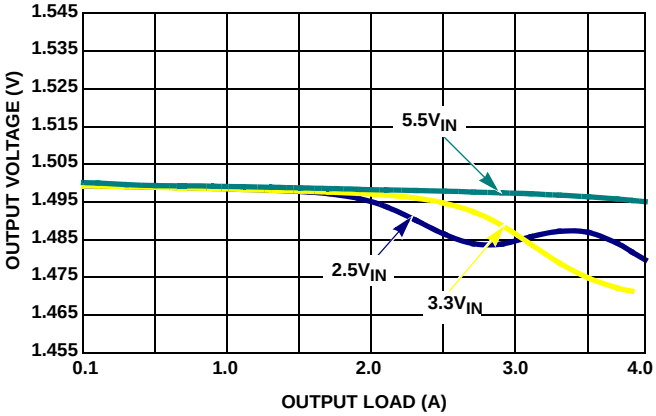


FIGURE 12. V_{OUT1} = 1.5V REGULATION vs LOAD

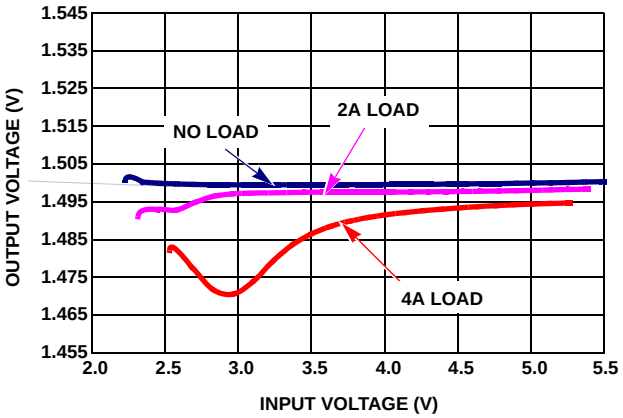


FIGURE 13. V_{OUT1} = 1.5V REGULATION vs V_{IN}

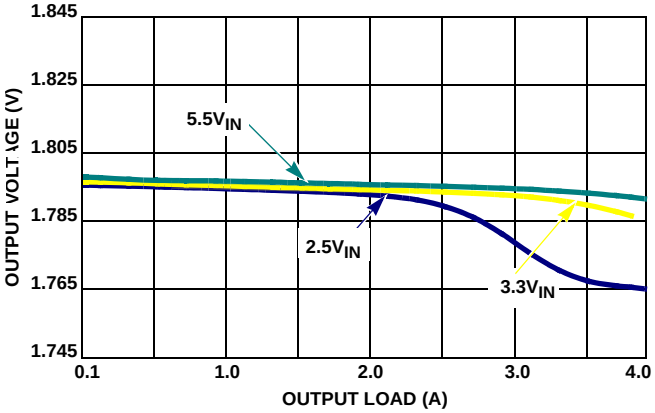


FIGURE 14. V_{OUT1} = 1.8V REGULATION vs LOAD

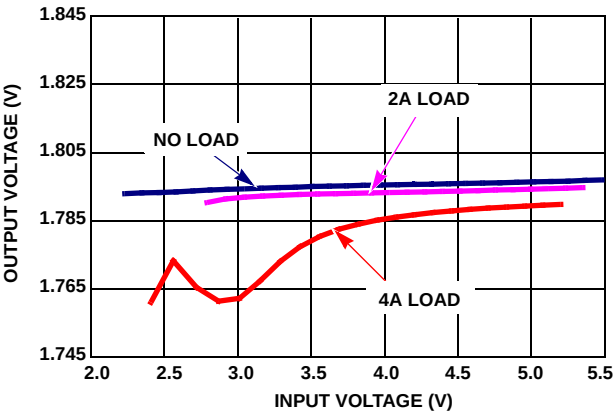


FIGURE 15. V_{OUT1} = 1.8V REGULATION vs V_{IN}

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 5V, I_{OUT1} = 4A, I_{OUT2} = 2A, T_A = -10°C to +100°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

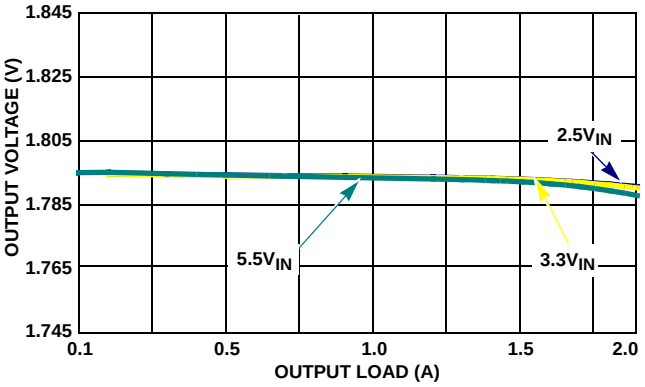


FIGURE 16. V_{OUT2} = 1.8V REGULATION vs LOAD

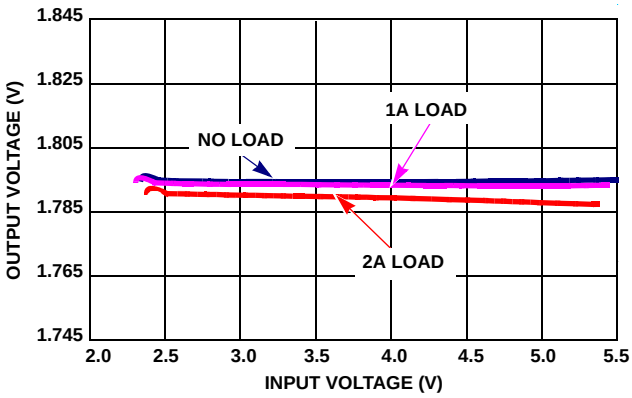


FIGURE 17. V_{OUT2} = 1.8V REGULATION vs VIN

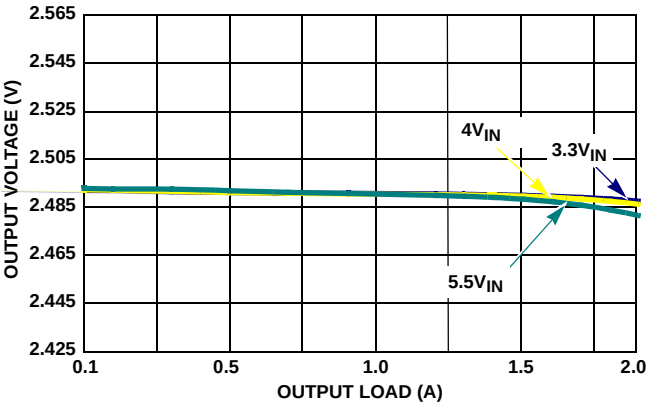


FIGURE 18. V_{OUT2} = 2.5V REGULATION vs LOAD

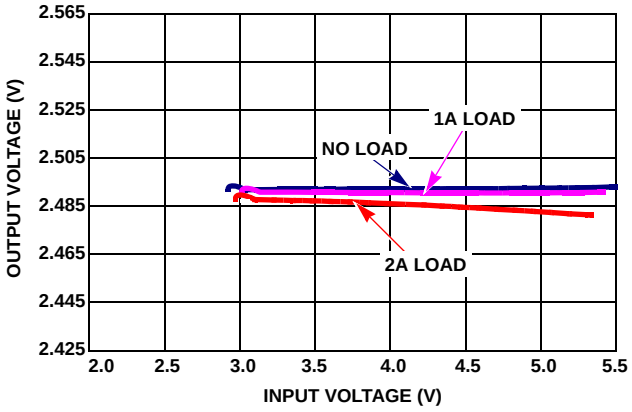


FIGURE 19. V_{OUT2} = 2.5V REGULATION vs VIN

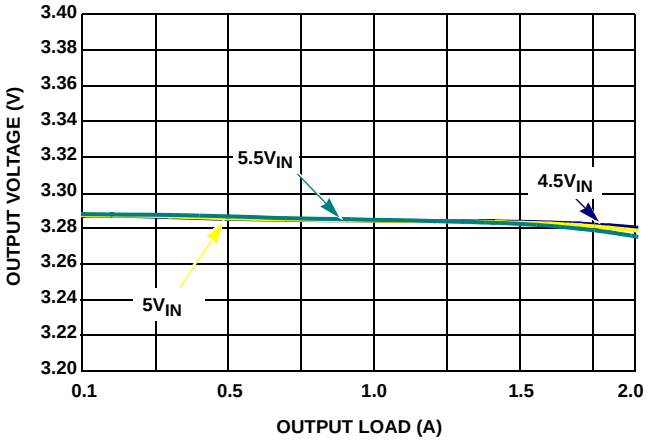


FIGURE 20. V_{OUT2} = 3.3V REGULATION vs LOAD

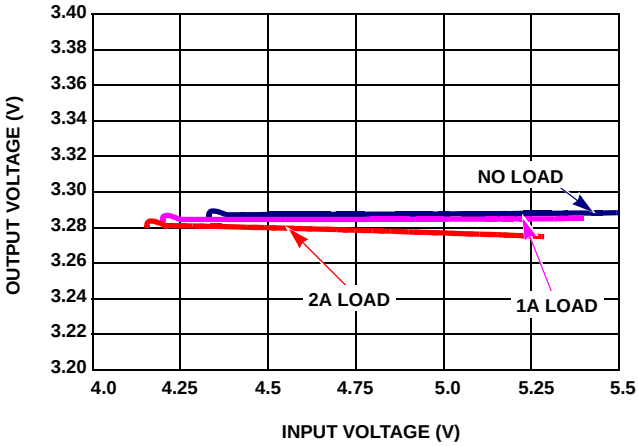


FIGURE 21. V_{OUT2} = 3.3V REGULATION vs VIN

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 5V, I_{OUT1} = 4A, I_{OUT2} = 2A, T_A = -10°C to +100°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

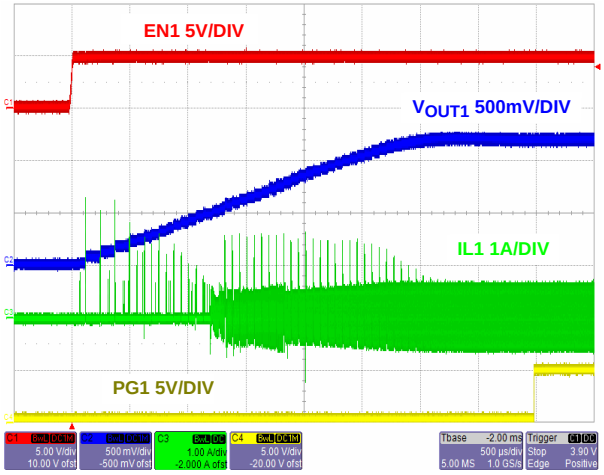


FIGURE 22. START-UP V_{OUT1} = 1.2V (NO LOAD)

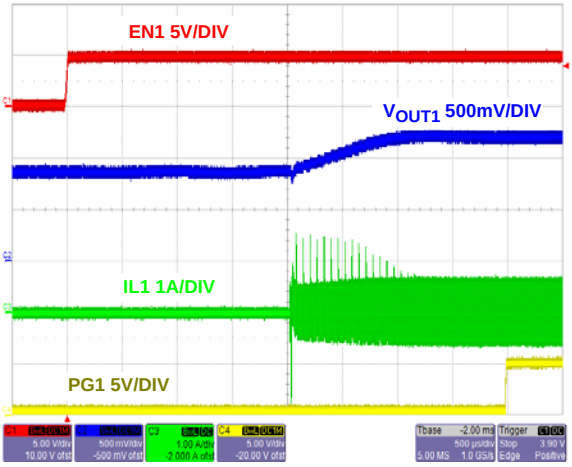


FIGURE 23. START-UP V_{OUT1} = 1.2V (UNDER PRE-BIASED)

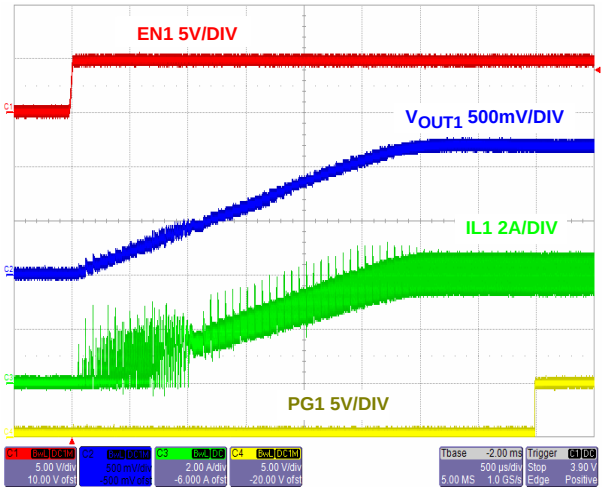


FIGURE 24. START-UP V_{OUT1} = 1.2V (FULL LOAD)

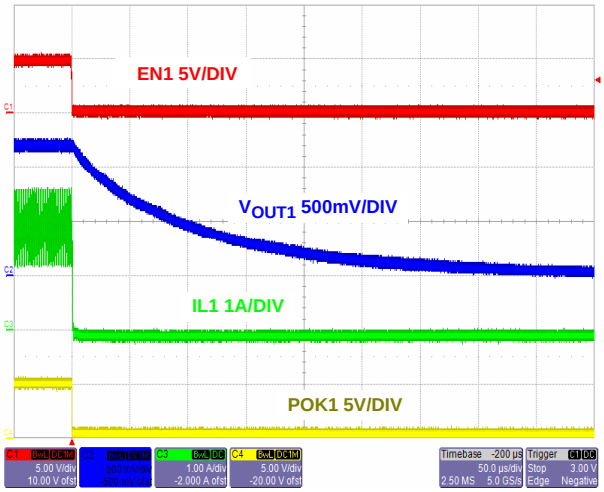


FIGURE 25. SHUTDOWN V_{OUT1} = 1.2V

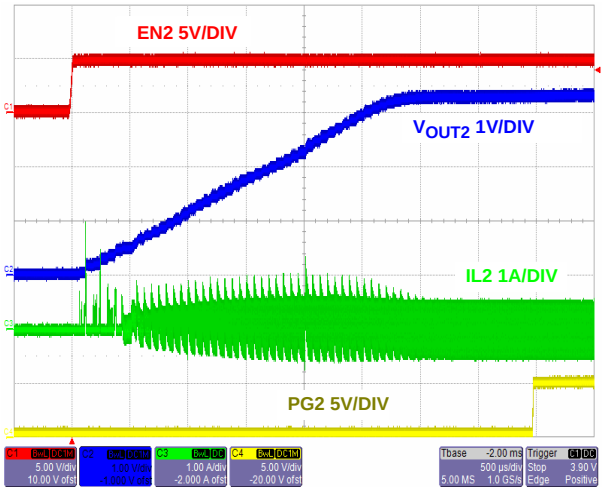


FIGURE 26. START-UP V_{OUT2} = 3.3V (NO LOAD)

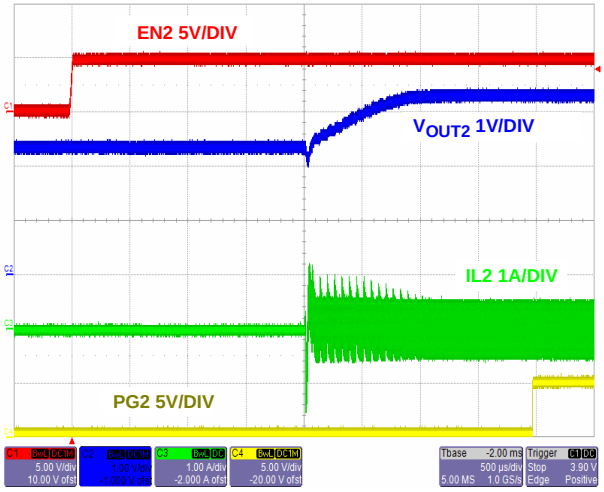


FIGURE 27. START-UP V_{OUT2} = 3.3V (UNDER PRE-BIASED)

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 5V, I_{OUT1} = 4A, I_{OUT2} = 2A, T_A = -10°C to +100°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

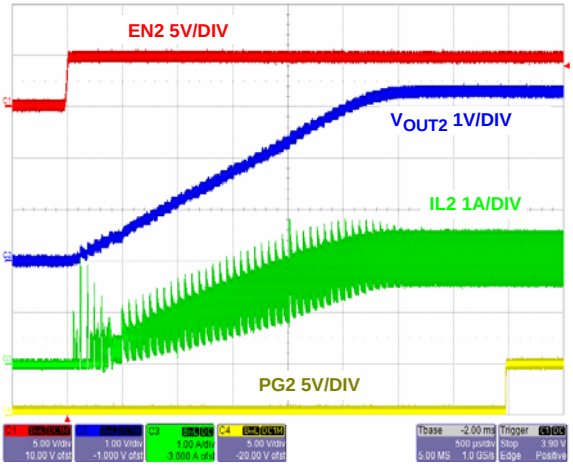


FIGURE 28. START-UP V_{OUT2} = 3.3V (FULL-LOAD)

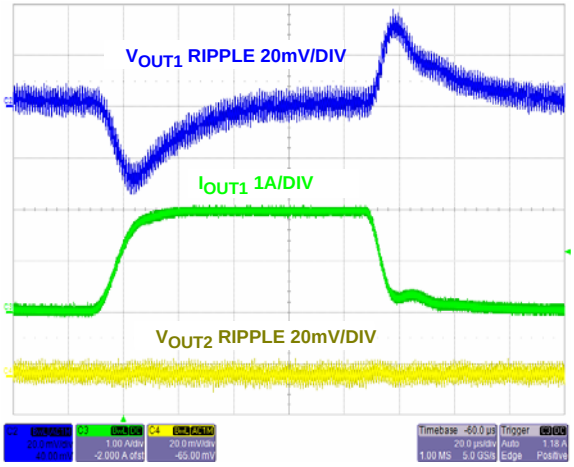


FIGURE 29. V_{OUT1} = 1.2V LOAD TRANSIENT

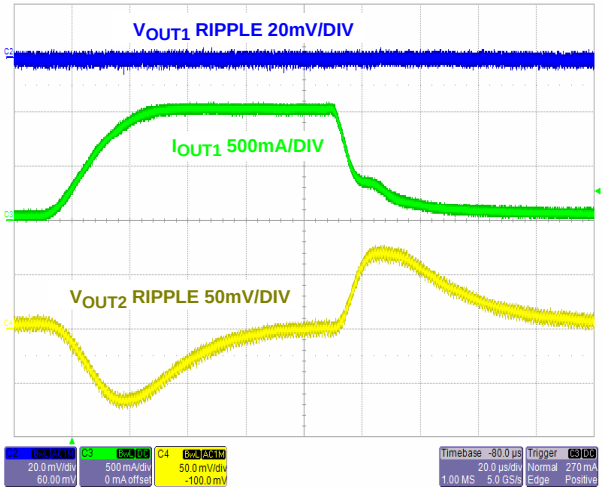


FIGURE 30. V_{OUT1} = 1.2V LOAD TRANSIENT

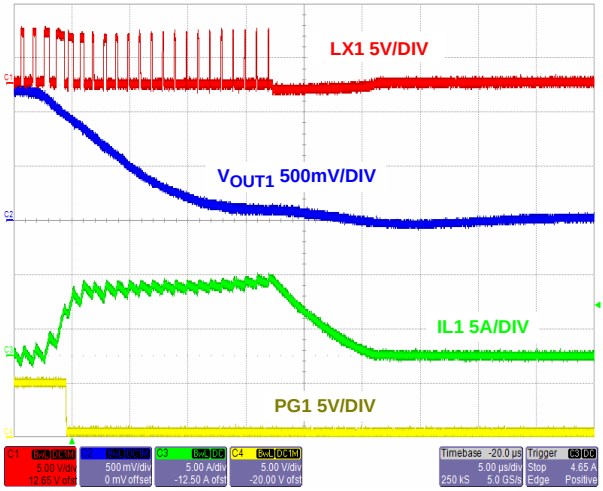


FIGURE 31. V_{OUT1} = 1.2V OUTPUT OVERCURRENT

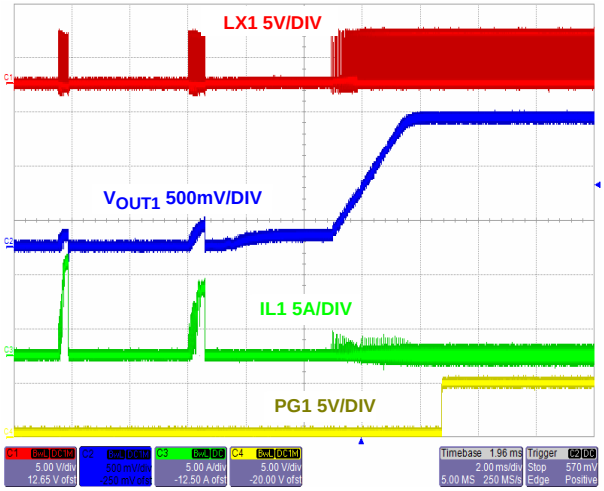


FIGURE 32. V_{OUT1} = 1.2V OUTPUT OVERCURRENT RECOVERY

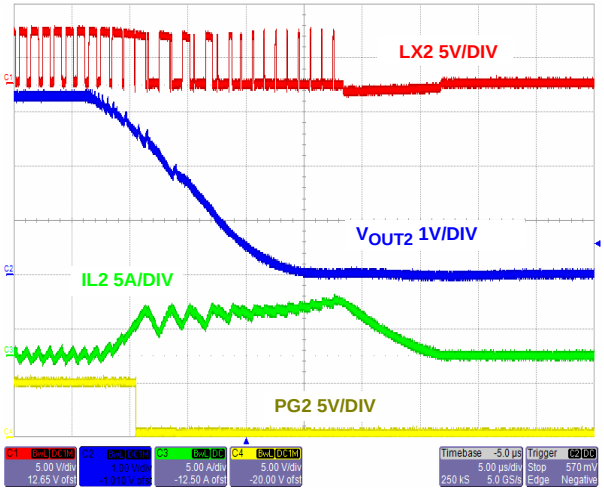


FIGURE 33. V_{OUT2} = 3.3V OUTPUT OVERCURRENT

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 5V, I_{OUT1} = 4A, I_{OUT2} = 2A, T_A = -10°C to +100°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

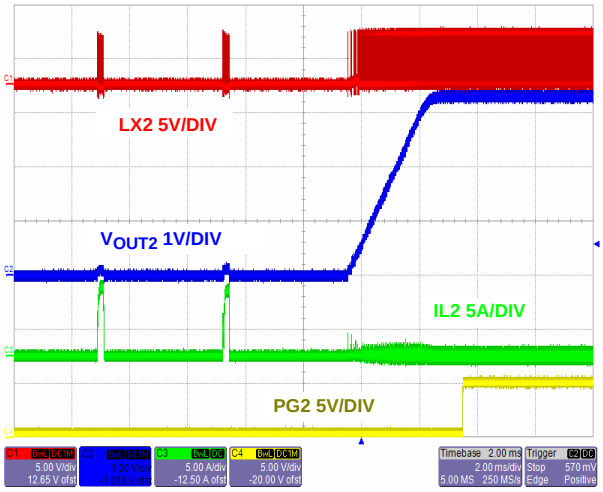
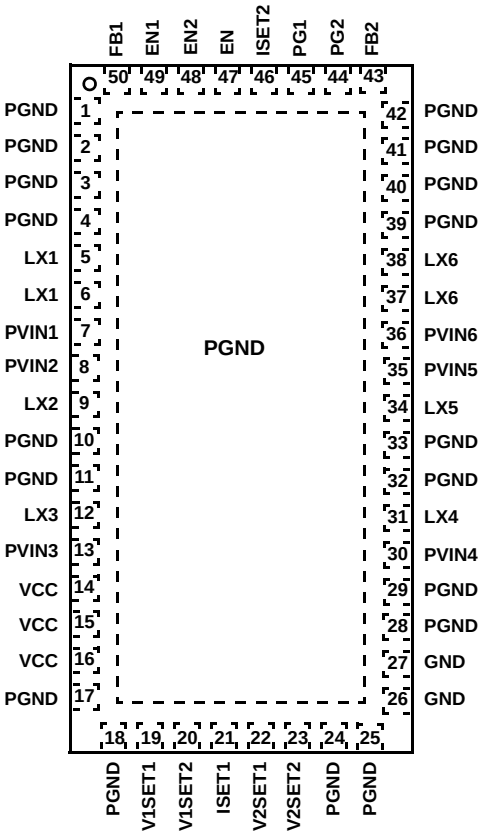


FIGURE 34. V_{OUT2} = 3.3V OUTPUT OVERCURRENT RECOVERY



Pin Descriptions

VCC

The bias supply input for the small signal circuitry. Connect this pin to the highest supply voltage available if two or more options are available. Locally filter this pin using a low ESL ceramic capacitor of 1µF or larger, and a 10Ω resistor.

PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, PVIN6

These pins are the power supply pins for the corresponding PWM power blocks. Associated power blocks must all tie to the same power supply. The power supply must fall in the range of 3V to 5.5V.

GND

Signal ground. All small signal components connect to this ground, which in turn connects to PGND at one point.

PGND

Power ground for the PWM power blocks and thermal relief for the package. The exposed pad must be connected to PGND and soldered to the PCB. Connect these pins closely to the negative terminal of input and output capacitors.

FB1, FB2

Voltage feedback input. Depending on the voltage selection pin settings, connect an optional resistor divider between V_{OUT} and GND for selection of a variable output voltage.

LX1, LX2, LX3, LX4, LX5, LX6

Switch node connection to inductor. This pin connects to the internal synchronous power MOSFET switches. The average voltage of this node is equal to the regulator output voltage.

EN

System enable for voltage monitoring with programmable hysteresis. This pin has a POR rising threshold of 0.6V. This enable is intended for applications where two or more input power supplies are used and bias rise time is an issue.

EN1, EN2

These pins are threshold-sensitive enable inputs for the individual PWM converters. These pins have low current (10µA) internal pull-ups to VCC. This pin disables the respective converter until pulled above a 1V rising threshold.

ISET1, ISET2

Power block configuration inputs. Select the proper state for each pin according to Table 1.

V1SET1, V1SET2, V2SET1, V2SET2

Output voltage configuration inputs. Select the proper state of each pin per the “Electrical Specifications” table.

PG1, PG2

Power-good output. Open drain logic output that is pulled to ground when the output voltage is outside regulation limits.

Functional Description

The ISL65426 is a monolithic, constant frequency, current-mode dual output buck converter controller with user configurable power blocks. Designed to provide a total DC/DC solution for FPGAs, CPLDs, core processors, and ASICs.

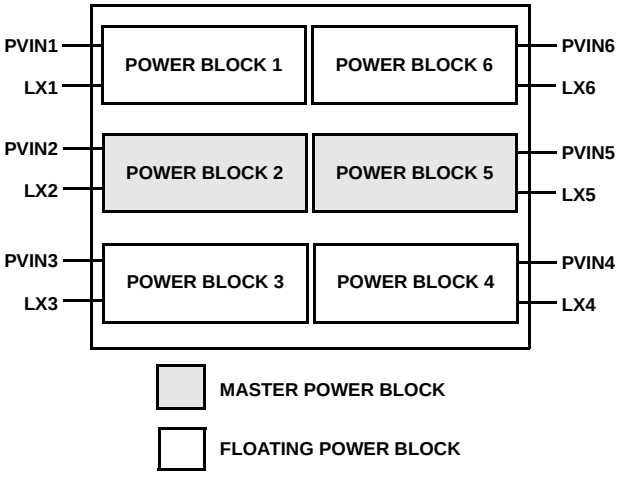


FIGURE 35. POWER BLOCK DIAGRAM

Power Blocks

A unique power block architecture allows partitioning of six 1A capable modules to support one of four power block configuration options. The block diagram in Figure 3 provides a top level view of the power block layout. One master power block is assigned to each converter output channel. Power Block 2 is allotted to converter Channel 1 and Power Block 5 to Channel 2. The master power blocks must not be tied together or the controller will not soft-start.

The remaining four floating power blocks can be partitioned in one of four valid states outlined in Table 1. The controller detects the programmed configuration based on the state of logic signals at pins ISET1 and ISET2. The controller checks the power block configuration versus the programmed configuration before the either converter can soft-start.

Each power block has a separate power supply connection pin, PVINx, and common channels must join these inputs to one input power supply. Common synchronous power switch connection points for each channel must be tied together and to an external inductor. See the “Typical Application Schematics” for pin connection guidance.

TABLE 1. POWER BLOCK CONFIGURATION

ISET1	ISET2	I_{OUT1}	CHANNEL 1 CONNECTIONS	I_{OUT2}	CHANNEL 2 CONNECTIONS
1	1	3A	LX1,LX2,LX3	3A	LX4,LX5,LX6
1	0	4A	LX1,LX2,LX3,LX4	2A	LX5,LX6
0	1	5A	LX1,LX2,LX3, LX4,LX6	1A	LX5
0	0	2A	LX1,LX2	4A	LX3,LX4,LX5,LX6
Invalid LX Configurations: SS Prevented					
X	X	1A	LX2	5A	LX1,LX3,LX4, LX5,LX6

Each power block has a scaled pilot device providing current feedback. The configuration pin settling determines how the controller handles separation and summing of the individual current feedback signals.

Main Control Loop

The ISL65426 is a monolithic, constant frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch is turned on at the beginning of each clock cycle. Current in the output inductor ramps up until the current comparator trips and turns off the top power MOSFET. The bottom power MOSFET turns on and the inductor current ramps down for the rest of the cycle.

The current comparator compares the output current at the ripple current peak to a current pilot. The error amplifier monitors V_{OUT} and compares it with the internal voltage reference. The error amplifier’s output voltage drives a proportional current to the pilot. If V_{OUT} is low the pilot’s current level is increased and the trip off current level of the output is increased. The increased current works to raise the V_{OUT} level into agreement with the voltage reference.

Output Voltage Programming

The feedback voltage applied to the inverting input of the error amplifier is scaled internally relative to the 0.6V internal reference voltage based on the state of logic signals at pins V1SET1, V1SET2, V2SET1 and V2SET2. The output voltage configuration logic decodes the 2-bit voltage identification codes into one of the discrete voltages shown

in Table 2. When each pin is pulled to GND by an internal 10µA pull-down, this default condition programs the output voltage to the lowest level. The pull-down prevents situations where a pin could be left floating for example (cold solder joint) from causing the output voltage to rise above the programmed level and damage a sensitive load device.

TABLE 2. OUTPUT VOLTAGE PROGRAMMING

VOUT1	V1SET1	V1SET2	VOUT2	V2SET1	V2SET2
1.8V	1	1	3.3V	1	1
1.5V	0	1	2.5V	0	1
1.2V	1	0	1.8V	1	0

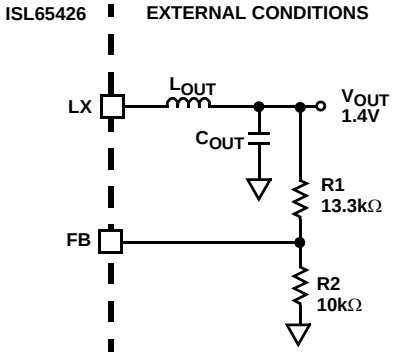


FIGURE 36. EXTERNAL OUTPUT VOLTAGE SELECTION

For designers requiring an output voltage level outside those shown in Table 2, the ISL65426 allows user programming with an external resistor divider (see Figure 36). First, both channel selection pins associated with that output channel must be tied to GND to set the internal reference to 0.6V. Next, the output voltage is set by an external resistive divider according to Equation 1. R_2 is selected arbitrarily, but 5kΩ or 10kΩ is usually a good starting point. The designer can configure the output voltage from 1V to 4V from a 5V power supply. Lower input supply voltages reduce the maximum programmable output voltage to 80% of the input voltage level.

$$R_1 = R_2 \cdot \frac{V_{OUT} - 0.6V}{0.6V} \quad \text{(EQ. 1)}$$

Switching Frequency

The controller features an internal oscillator running at a fixed frequency of 1MHz. The oscillator tolerance is ±20% over input bias and load range.

Operation Initialization

The ISL65426 initializes based on the state of three enable inputs (EN, EN1, EN2) and power-on reset (POR) monitors on VCC and PVINx inputs. Successful initialization of the controller prompts a one time power block configuration check. Verification of proper phase connections lead to a soft-start interval. The controller begins slowly ramping the output voltages based on the enable input states. Once the commanded output voltage is within the proper window of operation, the power-good signal corresponding to the active channel changes state from low to high indicating proper operation initialization.

Power-On Reset

The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at vital power supply input pins. These include the VCC and PVINx pins.

The VCC pins have a variable POR threshold based on the output voltage configuration pin configuration of VOUT2. If the configuration pins are set for 2.5V, the VCC POR rising threshold is typically 2.9V. The 3.3V configuration increases the VCC POR level to 4.3V. This variable rising threshold guarantees that the controller can properly switch the internal power blocks at the assigned output voltage levels.

The PVINx pins have a set POR rising threshold for all output voltage configurations. While the voltage on these pins are below this threshold (as defined in the “Electrical Specifications” table), the controller inhibits switching of the internal power MOSFETs.

Built-in hysteresis between the rising and falling thresholds insures that once enabled, the controller will not inadvertently toggle turn off unless the bias voltage drops substantially. While these pins are below the POR rising threshold, the synchronous power switch LX pins are held in a high-impedance state.

If additional POR control is required, a system enable input can be used to govern initialization, as described in the following section.

Enable and Disable

If the POR input requirements are met, the ISL65426 remains in shutdown until the voltage at the enable inputs rise above their enable thresholds. Independent enable inputs, EN1 and EN2, allow initialization of either buck converter channel separately, sequenced, or simultaneously. Both pins feature a 10µA pull-up, which will initialize both sides once the voltage at their respective pins exceeds the rising enable threshold, as defined in the “Electrical Specifications” table.

Both converters are governed by the presence of a system enable, EN. When two separate input supplies are used for each channel of power blocks or an external signal needs to govern the power-up sequence, the system enable provides a start-up sequencing mechanism.

The system enable features an internal 11µA pull-down, which is only active when the voltage on the EN pin is below the enable threshold. The current sink pulls the EN pin low. As VCC2 rises, the enable level is not set exclusively by the resistor divider from VCC2. With the current sink active, the

enable level is defined in Equation 2. R_1 is the resistor EN to VCC2 and R_2 is the resistor from EN to GND.

$$V_{ENABLE} = R_1 \cdot \left[\frac{0.6V}{R_2} + 10\mu A\right] + 0.6V \quad \text{(EQ. 2)}$$

Once the voltage at the EN pin reaches the enable threshold, the 10µA current sink turns off.

With the part enabled and the current sink off, the disable level is set by the resistor divider. The disable level is defined in Equation 3.

$$V_{DISABLE} = 0.6V \cdot \frac{R_1 + R_2}{R_2} \quad \text{(EQ. 3)}$$

The difference between the enable and disable levels provides the user with configurable hysteresis to prevent premature tripping.

To enable the controller, the system enable must be high, and one or both of the channel enables must be high. The POR circuitry must be satisfied for both VCC and PVINx inputs. Once these conditions are met, the controller immediately initiates a power block configuration check.

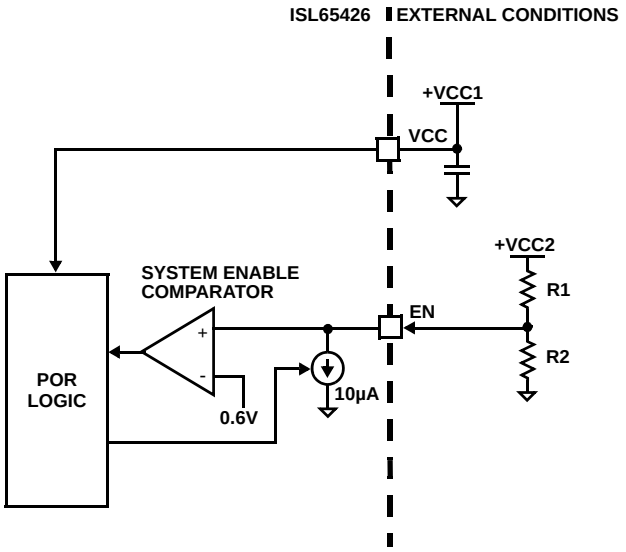


FIGURE 37. SYSTEM ENABLE INPUT

Power Block Configuration Check

After VCC exceeds its POR rising threshold, the controller decodes ISET1 and ISET2 states into one of four valid power block configurations (see Table 1). These pins are not checked again unless VCC falls below the POR falling threshold. The valid configuration is saved for comparison with the LX slave connectivity result, which is determined during the configuration check.

Once the POR and enable circuitry is satisfied, the controller initiates a configuration check. The master power block of output Channel 1 (Power Block 2) pulses high for 100ns. The configuration check circuitry detects which power blocks share a common LX connection and compares this to the decoded valid configuration. The master power block of output Channel 2 (Power Block 5) pulses, and again, the LX pins of the other non-master blocks are monitored. The common LX connections are checked versus the decoded valid configuration. Each floating power block has a pull-down active only during the configuration check to remove noise related false positive detections.

A successful configuration check initiates a soft-start interval 100µs after completion. Failing the configuration check, the controller will attempt a configuration check again 100µs after completing the first check cycle. The controller repeats the configuration check cycle every 100µs until a valid configuration is detected or the controller is powered down. Once successful, the configuration check is not implemented again until VCC falls below the POR falling threshold. Re-enabling the controller after a successful configuration check will immediately initiate a soft-start interval.

Soft-start Interval

Once the controller is enabled and power block configuration is successful, the digital soft-start function clamps the error amplifier reference. The digital soft-start circuitry ramps the output voltage by stepping the reference up gradually over a fixed interval of 4ms. The controlled ramp of the output voltage reduces the in-rush current during startup.

Power-good Signal

Each power-good pin (PG1, PG2) is an open-drain logic output that indicates when the converter output voltage is within regulation limits. The power-good pins pull low during shutdown and remain low when the controller is enabled. After a successful converter channel soft-start, the power-good pin signal associated with that channel releases and the power-good pin voltage rises with an external pull-up resistor. The power-good signal transitions low immediately upon the removal of individual channel or system enable.

The power-good circuitry monitors both output voltage FB pins and compares them to the rising and falling limits shown in the “Electrical Specifications” table. If either channel’s feedback voltage exceeds the typical rising limit of 115% of the reference voltage, the power-good pin pulls low. The power-good pin continues to pull low until the feedback voltage recovers down by a typical of 110% of the reference voltage. If either channel’s feedback voltage drops below a typical of 85% of the reference voltage, the power-good pin related to the offending channel(s) pulls low. The power-good pin continues to pull low until the feedback voltage rises to within 90% of the reference voltage. The power-good pin then releases and signals the return of the output voltage within the power-good window.

Fault Monitoring and Protection

The ISL65426 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to the controller and external

load device. Individual power-good indicators provide options for linking to external system monitors.

Undervoltage Protection

Separate hysteretic comparators monitor the feedback pin (FB) of each converter channel. The feedback voltage is compared to a set undervoltage (UV) threshold based on the output voltage selected. Once one of the comparators trip indicating a valid UV condition, a 4-bit UV counter increments. If both channel comparators detect an UV condition during the same switching cycle, the 4-bit counter increments twice. Once the 4-bit counter overflows, the UV protection logic shuts down both regulators.

The comparator is reset if the feedback voltage rises back up above the UV threshold plus a specified amount of hysteresis outlined in the “Electrical Specifications” table. If both converter channels experience an UV condition and one rises back within regulation, then the counter continues to progress toward overflow.

Overvoltage Response

If the output voltage exceeds the overvoltage (OV) level for the power-good signal, the controller will fight this condition by actively trying to regulate the output voltage back down to the reference level. This method of fighting the rise in output voltage is limited by the reverse current capability of the total number of power blocks associated with the output. The approximate reverse current capability of each power block is 0.5A. The power-good signal will drop indicating the output voltage is out of specification. This signal will not transition high again until the output voltage has dropped below the falling PGOOD OV threshold.

Overcurrent Protection

A pilot device is integrated into the upper device structure of each master power block. The pilot device samples current through the master power block upper device each cycle. This channel current feedback is scaled based on the state of the ISET1 and ISET2 pins. The channel current information is compared to an overcurrent (OC) limit based on the power block configuration. Each 1A power block tied to the master power block increases the OC limit by 2A. For example, if both masters have two slaves associated with each of them then the OC limit for each output is 6A for a 3A configuration.

If the sampled current exceeds the OC threshold, a 4-bit OC up/down counter increments by one LSB. If the sampled current falls below the OC threshold before the counter overflows, the counter is reset. If both regulators experience an OC event during the same cycle, the counter increments twice. Once the OC counter reaches 1111, both channels are shutdown. If both channels fall below the overcurrent limit during the same cycle, the OC counter is reset.

Once in shutdown, the controller enters a delay interval, equivalent to the SS interval, allowing the die to cool. The OC counter is reset entering the delay interval. The protection logic initiates a normal SS internal once the delay interval ends. If the outputs both successfully soft-start, the power-good signal goes high and normal operation continues. If OC conditions continue to exist during the SS interval, the OC counter must overflow before the controller shutdowns both outputs again. This hiccup mode continues indefinitely until both outputs soft-start successfully.

Note: It is recommended to add a Schottky diode of adequate rating from LX1 to PGND and from LX5 to PGND to avoid severe negative ringing that can disturb the OC counter.

Thermal Monitor

Thermal-overload protection limits total power dissipation in the ISL65426. An internal thermal sensor monitors die temperature continuously. If controller junction temperature exceeds +150°C, the thermal monitor commands the POR circuitry to shutdown both channels and latch-off. The POR latch is reset by cycling VCC to the controller.

Component Selection Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides a complete reference design that includes schematics, a bill of materials and example board layout.

Output Filter Design

The output inductor and the output capacitor bank together form a low-pass filter responsible for smoothing the pulsating voltage at the phase node. The output filter also must provide the transient energy until the regulator can respond. Due to its inherent low bandwidth as compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

OUTPUT CAPACITOR SELECTION

The critical load parameters in choosing the output capacitors are the maximum size of the load step (ΔI), the load-current slew rate (di/dt), and the maximum allowable output voltage deviation under transient loading (ΔV_{MAX}). Capacitors are characterized according to their capacitance, ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. Neglecting the contribution of inductor current and

regulator response, the output voltage initially deviates by an amount shown in Equation 4.

$$\Delta V \approx \left[ESL \times \frac{di}{dt}\right] + [ESR \times \Delta I] \quad \text{(EQ. 4)}$$

The filter capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation ΔV is less than the maximum allowable ripple.

The recommended load capacitance can be estimated using Equation 5.

$$C_{OUT} = 0.5 \times \text{Number of LX channels used} \times 150\mu F \times \frac{1.8V}{V_{OUT}} \quad \text{(EQ. 5)}$$

The internal compensation scheme assumes low-ESR output capacitors. It is recommended to only use specialty polymer or ceramic capacitors with ESRs of 10mΩ or lower. Care also needs to be taken to ensure that the dielectric of the capacitor used will work reliably in the entire temperature range of the application.

Design Example:

Consider an output voltage of 1.2V, with LX1, LX2, LX3 and LX4 connected. The output capacitance required would be:

$$C_{OUT} = 0.5 \bullet 4 \bullet 150\mu F \bullet \frac{1.8V}{1.2V} = 450\mu F \quad \text{(EQ. 6)}$$

A 330µF specialty polymer capacitor in parallel with three 47µF X7R ceramic capacitors would be the recommended choice of output filter.

OUTPUT INDUCTOR SELECTION

Once the output capacitors are selected, the maximum allowable ripple voltage, V_{PPMAX}, determines the lower limit on the inductance. See Equation 7.

$$L \geq ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{f_s \times V_{IN} \times V_{PP_{MAX}}}\right] \quad \text{(EQ. 7)}$$

Since the output capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 8 gives the upper limit on output inductance for the cases when the trailing edge of the current transient causes the greater output voltage deviation than the leading edge. Equation 9 addresses the leading edge. Normally, the trailing edge dictates the inductance selection because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and inductance should be governed based on the lower of the two results. In each equation, L is the output inductance and C is the total output capacitance.

$$L \leq \frac{2 \cdot C \cdot V_O}{(\Delta I)^2}\left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 8)}$$

$$L \leq \frac{(1.25) \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right]\left(V_{IN} - V_O\right) \quad \text{(EQ. 9)}$$

The other concern when selecting an output inductor is the internally set current mode slope compensation. Designs should not allow inductor ripple currents below 0.125 times the maximum output current to prevent regulation issues.

It is recommended to use a 30% peak-to-peak ripple current value to calculate out the inductance required for the application. Accordingly, the inductance estimated using Equation 10 below would fall between the minimum inductance value calculated in Equation 7 and the maximum values determined from Equations 8 and 9.

$$L @ \left[\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_s \times \frac{I_{OUT_{MAX}}}{3}}\right] \quad \text{(EQ. 10)}$$

Input Capacitor Selection

Input capacitors are responsible for sourcing the AC component of the input current flowing into the switching power devices. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the switching power devices, which is related to duty cycle. The maximum RMS current required by the regulator is closely approximated by Equation 11.

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT_{MAX}}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_s} \times \frac{V_{OUT}}{V_{IN}}\right)^2\right)} \quad \text{(EQ. 11)}$$

The important parameters to consider when selecting an input capacitor are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage ratings above the maximum input voltage. The rated voltage rating should be at least 1.25 times greater than the maximum input voltage while using aluminum electrolytic capacitors, and about 2 times the maximum input voltage to account for capacitance derating in case of ceramic capacitors. The capacitor RMS current rating should be higher than the largest RMS current required by the circuit.

The ISL65426 needs a minimum effective input capacitance of 70µF with low ESR for stable operation.

Layout Considerations

Careful printed circuit board (PCB) layout is critical in high frequency switching converter design. Current transitions from one device to another at this frequency induce voltage spikes across the interconnecting impedances and parasitic elements. These spikes degrade efficiency, lead to device overvoltage stress, radiate noise into sensitive nodes, and increase thermal stress on critical components. Careful component placement and PCB layout minimizes the voltage spikes in the converter.

The following multi-layer printed circuitry board layout strategies minimize the impact of board parasitics on converter performance and optimize the heat-dissipating capabilities of the printed circuit board. This section highlights some important practices which should not be overlooked during the layout process. Figure 38 provides a top level view of the critical components, layer utilization, and signal routing for reference.

Component Placement

Determine the total implementation area and orient the critical switching components first. These include the controller, input and output capacitors, and the output inductors. Symmetry is very important in determining how available space is filled and depends on the power block configuration selected. The controller must be placed equidistant from each output stage with the LX or phase connection distance minimized.

An output stage consists of the area reserved for the output inductor, and input capacitors, and output capacitors for a single channel. Place the inductor such that one pad is a minimal distance from the associated phase connection. Orient the inductor such that the load device is a short distance from the other pad. Placing the input capacitors a minimal distance from the PVIN pins prevents long distances from adding too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductor and the load device, while keeping them in close proximity. Care should be taken not to add inductance through long trace lengths that could cancel the usefulness of the low inductance components. Keeping the components in tight proximity will help reduce parasitic impedances once the components are routed together.

Bypass capacitors, C_{BP}, supply critical filtering and must be placed close to their respective pins. Stray trace parasitics will reduce their effectiveness, so keep the distance between the VCC bias supply pad and capacitor pad to a minimum.

Plane Allocation

PCB designers typically have a set number of planes available for a converter design. Dedicate one solid layer, (usually an internal layer underneath the component side of the board), for a ground plane and make all critical component ground connections with vias to this layer.

One additional solid layer is dedicated as a power plane and broken into smaller islands of common voltage. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit board layers for small signal wiring and additional power or ground islands as required.

Signal Routing

If the output stage component placement guidelines are followed, stray inductance in the switch current path is minimized along with good routing techniques. Great attention should be paid to routing the PHASE plane since high current pulses are driven through them. Stray inductance in this high-current path induces large noise voltages that couple into sensitive circuitry. By keeping the PHASE plane small, the magnitude of the potential spikes is minimized. It is important to size traces from the LX pins to the PHASE plane as large and short as possible to reduce their overall impedance and inductance.

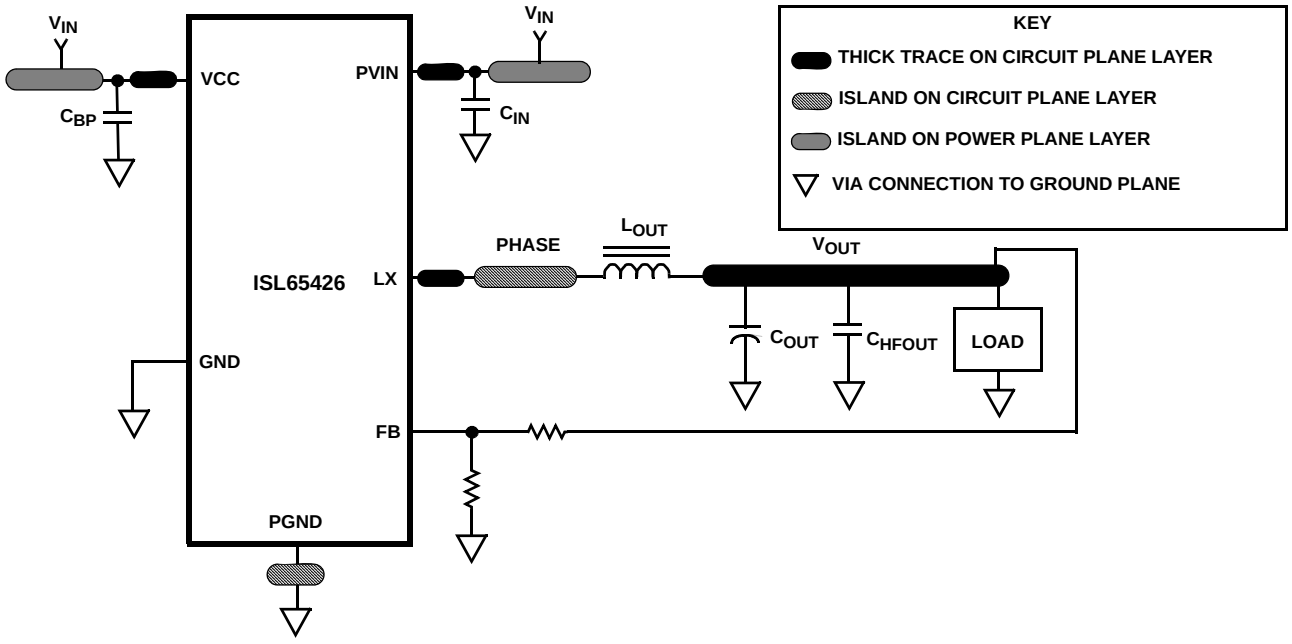


FIGURE 38. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

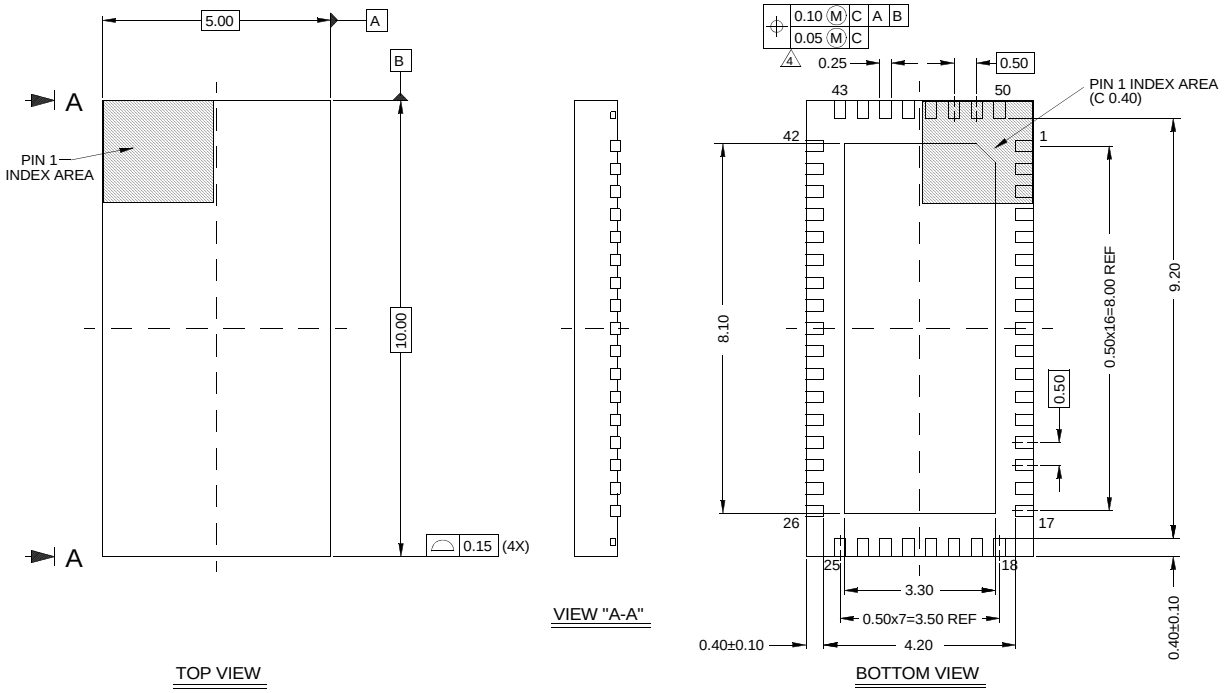
Sensitive signals should be routed on different layers or some distance away from the PHASE plane on the same layer. Crosstalk due to switching noise is reduced into these lines by isolating the routing path away from the PHASE plane. Layout the PHASE planes on one layer, usually the top or bottom layer, and route the voltage feedback traces on another remaining layer.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal PGND pad of the ISL65426 to the ground plane with multiple vias is recommended. This heat spreading allows the IC to achieve its full thermal potential. If possible, place the controller in a direct path of any available airflow to improve thermal performance.

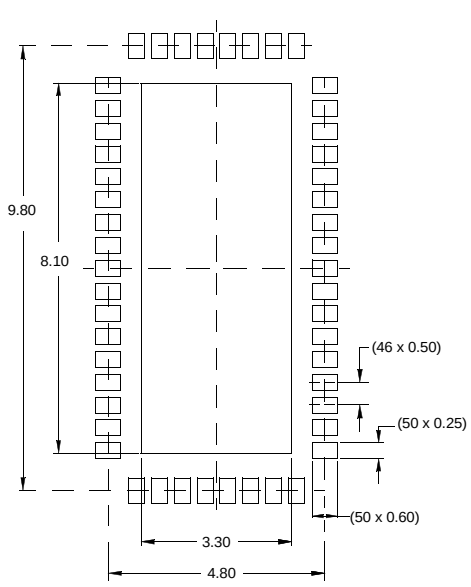
L50.5x10

50 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 7/06

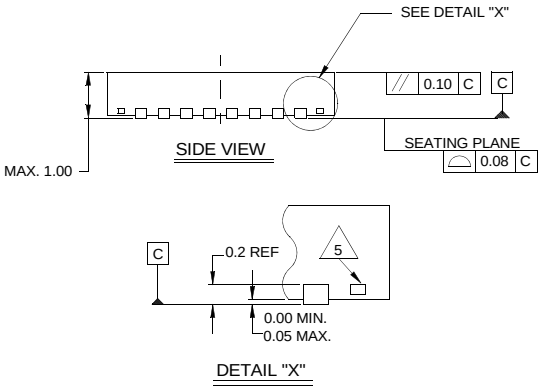


TOP VIEW

BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

DETAIL "X"

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MM.
2. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05
   ANGULAR ±2×
3. DIMENSIONING AND TOLERANCE PER ASME Y 14.5M-1994.
4. DIMENSION LEAD WIDTH APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.23MM AND 0.28MM FROM THE TERMINAL TIP.
5. TIEBAR SHOWN (if present) IS A NON-FUNCTIONAL FEATURE

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